CLAIMS

1. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

2. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

a single intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first semiconductor die and said second semiconductor die such that a first surface of said intermediate substrate faces said first semiconductor die and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through, and

one of said first semiconductor die and said second semiconductor die is positioned such that said conductive bond pad on one of said first and second active surfaces is aligned with said passage;

a printed circuit board positioned such that a first surface of said printed circuit board faces said intermediate substrate;

a plurality of topographic contacts extending from said intermediate substrate to said first surface of said printed circuit board; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

3. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

an additional substrate comprising a network of conductive contacts formed thereon, said additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate, wherein

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said second surface of said additional substrate and such that said conductive line extends through a space defined between said second surface of said additional substrate and said first surface of said printed circuit board; and

a plurality of topographic contacts extending from said second surface of said additional substrate to said first surface of said printed circuit board.

4. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate,

said intermediate substrate defines a passage there through,

said second semiconductor die is secured to said second surface of said intermediate substrate such that said conductive bond pad of said second semiconductor die is aligned with said passage, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said first surface of said intermediate substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said second surface of said intermediate substrate and such that said second semiconductor die is positioned between said printed circuit board and said intermediate substrate;

a plurality of topographic contacts extending from said second surface of said intermediate substrate to said first surface of said printed circuit board; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

5. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die, wherein

said intermediate substrate defines a passage there through,

said first semiconductor die is secured to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with said passage, and

said first semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

an additional substrate comprising a network of conductive contacts formed thereon, said additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die, wherein

said additional substrate defines an additional passage there through,

said second semiconductor die is secured to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with said additional passage, and

said second semiconductor die is electrically coupled to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said second surface of said additional substrate and such that said conductive line extends through a space defined between said second surface of said additional substrate and said first surface of said printed circuit board;

a plurality of topographic contacts extending from said second surface of said additional substrate to said first surface of said printed circuit board; and

at least one decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of

said first semiconductor die,

said second semiconductor die,

a topographic contact conductively coupled to said first semiconductor die, and

a topographic contact conductively coupled to said second semiconductor die.

6. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said second active surface to said second surface of said intermediate substrate;

a printed circuit board positioned such that a first surface of said printed circuit board faces said second surface of said intermediate substrate and such that said second semiconductor die is positioned between said printed circuit board and said intermediate substrate; and

a plurality of topographic contacts extending from said second surface of said intermediate substrate to said first surface of said printed circuit board.

7. A printed circuit board assembly as claimed in claim 6 further comprising a decoupling capacitor conductively coupled to at least one of said first and second semiconductor dies,

wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of said topographic contact extending from said first active surface to said first surface of said intermediate substrate.

8. A printed circuit board assembly comprising:

a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

an intermediate substrate comprising a network of conductive contacts formed thereon, said intermediate substrate positioned between said first active surface of said first semiconductor die and said second active surface of said second semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second active surface, wherein

said first semiconductor die is electrically coupled to said intermediate substrate by at least one topographic contact extending from said first active surface to said first surface of said intermediate substrate,

said intermediate substrate defines a passage there through,

said second semiconductor die is secured to said second surface of said intermediate substrate such that said conductive bond pad of said second semiconductor die is aligned with said passage, and

said second semiconductor die is electrically coupled to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said first surface of said intermediate substrate;

at least one decoupling capacitor mounted to said first surface of said intermediate substrate and conductively coupled to at least one of said first and second semiconductor dies, wherein a thickness dimension of said decoupling capacitor is accommodated in a space defined

by a thickness dimension of a topographic contact conductively coupled to a conductive contact on said first surface of said intermediate substrate; and

a heat sink including a cap portion and a peripheral portion, wherein

said cap portion is thermally coupled to a major surface of at least one of said first and second semiconductor dies, and

said peripheral portion engages a mounting zone defined by a lateral dimension of said intermediate substrate extending beyond a periphery of at least one of said first and second semiconductor dies.

9. A printed circuit board assembly as claimed in claim 1 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said semiconductor dice.

10. A printed circuit board assembly as claimed in claim 1 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to one of said semiconductor dice.

11. A printed circuit board assembly as claimed in claim 4 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said semiconductor dice.

12. A printed circuit board assembly as claimed in claim 4 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to one of said semiconductor dice.

13. A printed circuit board assembly as claimed in claim 5 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of one of said semiconductor dice.

14. A printed circuit board assembly as claimed in claim 5 wherein said thickness dimension of said decoupling capacitor is accommodated in a space defined by a thickness dimension of a topographic contact conductively coupled to one of said semiconductor dice.

15. A printed circuit board assembly as claimed in claim 1, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

16. A printed circuit board assembly as claimed in claim 2, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

17. A printed circuit board assembly as claimed in claim 3, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

18. A printed circuit board assembly as claimed in claim 4, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

19. A printed circuit board assembly as claimed in claim 5, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

20. A printed circuit board assembly as claimed in claim 6, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

21. A printed circuit board assembly as claimed in claim 7, wherein said printed circuit board assembly is resident in a computer system comprising a programmable controller and at least one memory unit, wherein said memory unit comprises said printed circuit board assembly.

22. A method of stacking a plurality of semiconductor die comprising:

providing a first semiconductor die defining a first active surface, said first active surface including at least one conductive bond pad;

providing a second semiconductor die defining a second active surface, said second active surface including at least one conductive bond pad;

positioning an intermediate substrate comprising a network of conductive contacts formed thereon between said second semiconductor die and said first active surface of said first semiconductor die such that a first surface of said intermediate substrate faces said first active surface and such that a second surface of said intermediate substrate faces said second semiconductor die;

securing said first semiconductor die to said first surface of said intermediate substrate such that said conductive bond pad of said first semiconductor die is aligned with a passage formed in said intermediate substrate;

electrically coupling said first semiconductor die to said intermediate substrate by at least one conductive line extending from said conductive bond pad of said first semiconductor die through said passage defined in said intermediate substrate and to a conductive contact on said second surface of said intermediate substrate;

providing an additional substrate comprising a network of conductive contacts formed thereon, said additional substrate positioned such that a first surface of said additional substrate faces said second active surface of said second semiconductor die and such that said first surface of said additional substrate opposes said second surface of said intermediate substrate;

securing said second semiconductor die to said first surface of said additional substrate such that said conductive bond pad of said second semiconductor die is aligned with an additional passage formed in said additional substrate;

electrically coupling said second semiconductor die to said additional substrate by at least one conductive line extending from said conductive bond pad of said second semiconductor die through said additional passage defined in said additional substrate and to a conductive contact on a second surface of said additional substrate;

positioning a printed circuit board such that a first surface of said printed circuit board faces said second surface of said additional substrate and such that said conductive line extends through a space defined between said second surface of said additional substrate and said first surface of said printed circuit board; and

forming a plurality of topographic contacts extending from said second surface of said additional substrate to said first surface of said printed circuit board.